Systems-On-A-Chip
Architecture, Design, Fabrication and Test

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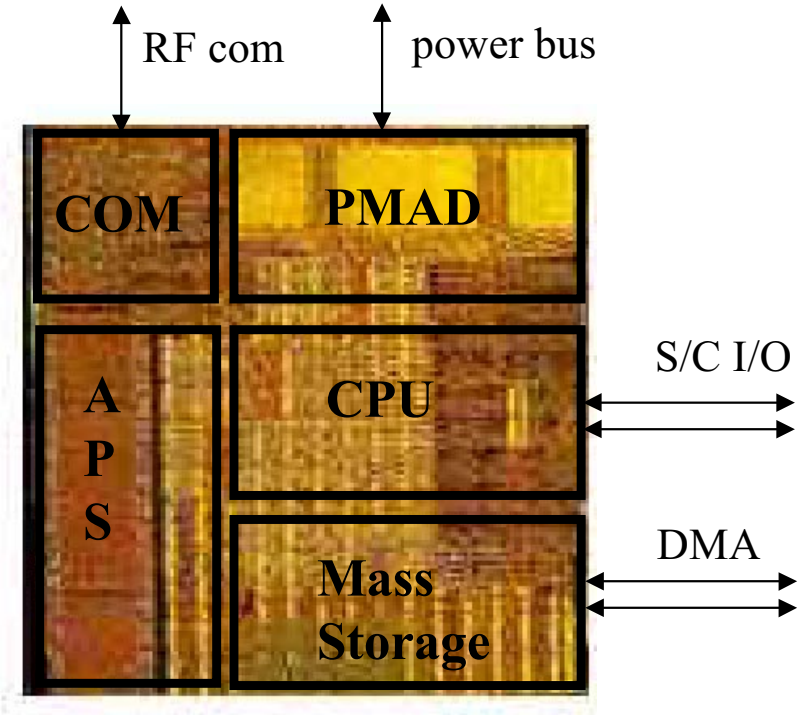
Outline

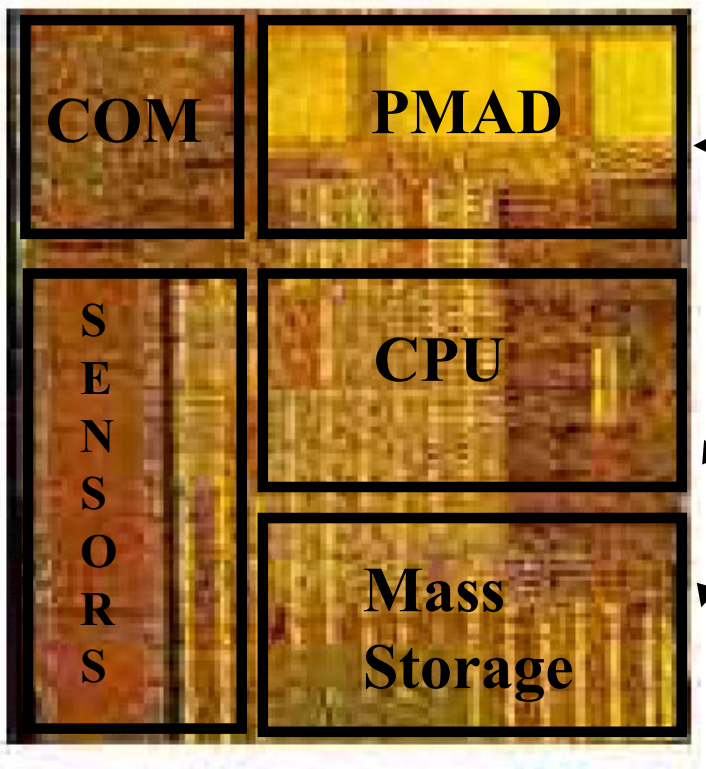
1. Introduction
   - SOAC Program, Vision and Challenges
2. System-On-A-Chip Technology
   - System Architecture Design
   - Reusable IP Based Design Method and Tool
   - Fabrication and Test
3. Experimental SOAC Chips:
   - Camera-on-a-chip
   - Neurocomputer-on-a-chip
   - Microcomputer-on-a-chip
   - Smart Vision System-on-a-chip
4. Future Work

SOAC-Vision

- Definition:
  - Highly capable, autonomous avionics system which includes CPU, mass memory, power management and distribution, telecomm, and sensors; all integrated into a single monolithic unit.
- Benefits:
  - Volume/Mass reduction
  - Improved performance and reliability
  - Power reduction
- Applications:
  - Spacecraft
    - Micro Spacecraft
    - Science Craft
    - Micro Probe
  - Micro and Nano Rovers
  - Aerobots



SOAC-Technical Challenges



•Miniaturization-RF
•Integration-RF
•Integration of optical com.

•Miniaturization
•Passive components
•Low power

•Integration of devices and integrated circuits with MEMS.

•Integration of processors and memory devices.
•Merging of individual designs

General challenges:

•Different design techniques and design tools (digital, analog, mixed, rf, optical, MEMS)
•Ultra low power devices and architectures
•Unified device fabrication technology-SOI CMOS, SOI MOSFET, SOI SI based memories, SiGe
•Testing of the system on a chip
•Reliability
•Intellectual Property related issues
•Successful partnership with industry for system on a chip fabrication

The SOAC Complexity and Challenge

Source: SIA Report 1997

Year	1997	1999	2001	2003	2005
Technology Life Cycle (Microns)	0.25	0.18	0.15	0.13	
Packing Density (Trans/sq. cm)	8 M	14M	16M	24M	
Chip Size (sq. mm)	300	340	385	430	
Clocking Freq. (MHz)	300	500	600	700	
RCL Product	=> narrow conductors and spacing RCL => interlayer dielectric Ci				

SOAC Design Challenge => Reusable IP cores based design method and tool needed

EDA Tool Challenge => An end-to-end EDA tool for hundred-million transistor chip design

SOAC Test Challenge => New BIST and DFT techniques needed
=> New fault models and failure analysis needed

Test Instrument Challenge => High frequency, high-pin-count probes and sockets needed
=> High sample rate, low noise mixed-signal test instruments needed

Proposed Solutions for SOAC Design Challenge: Reusable IP Based SOAC Design

IP Provider → SOAC Integrator

Reusable IP Creation

- VHDL- Verilog
- RTL
- Gate
- Transistor
- Layout
- Test Vectors

Export

Reusable IP Requirements:
- Secure
- Portable
- Repeatable
- Usability
- Performance
- Consistency

Advantages:
Recurring costs are kept low through the use of reusable IP that can be designed once and then employed in many SOACs.

System Design
Algorithm and architecture design and partitioning
IP selection and system simulation

Logic Design
Target function and performance
HDL development and synthesis
Block refinement and interconnect
Block modification and verification

Test Design
Test method and test bench
Test structures, vectors, ATG
Test structure insertion
Scan chain reordering
Production test creation

Physical Design
Target Power, packaging and loading
Floorplan, estimated block size, loading
Timing/Size/Power/Cluster
Post-layout up-dates for timing/ size / power
Silicon prototype and certification

System/Chip Integration and Test

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Proposed Solutions for SOAC Test Challenge: New BIST and DFT techniques and Test Instrument

- New BIST and DFT techniques needed for better controllability and observability.
- New fault models and failure analysis needed for advanced multilevel-metal ICs.
- High frequency, high-pin-count probes and sockets needed
- High sample rate, low noise mixed-signal test instruments needed
- Tools and rules needed to automatically generate and check the test programs.

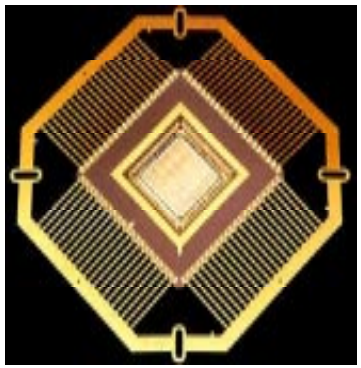
SOAC Chip Development Team - Team SOAC

(Proposed)

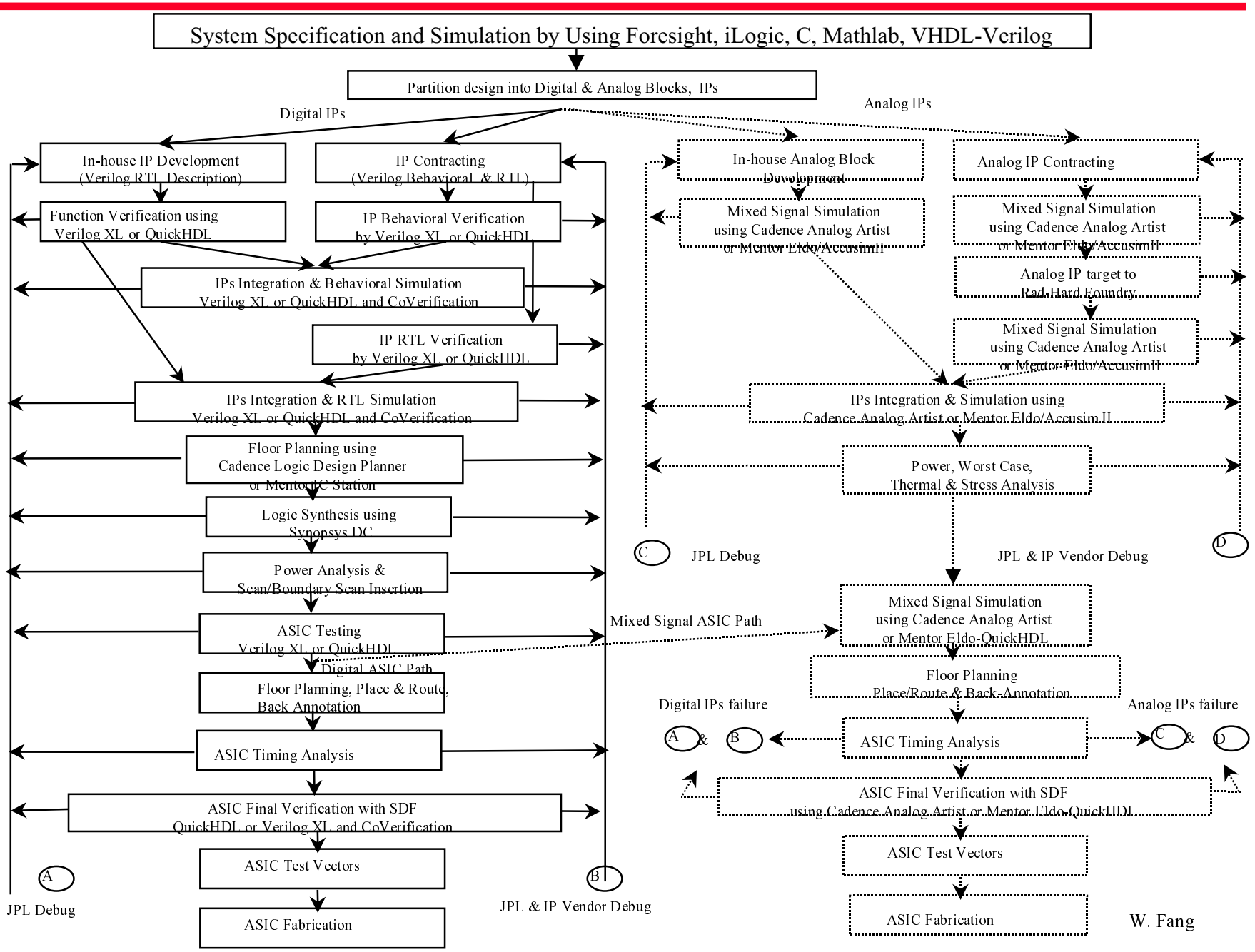
• Team SOAC is a team of VLSI Microsystems specialists which interface with various projects to provide system-on-a-chip solutions.

•Team SOAC is composed of a couple core members each representing a particular element of the System-On-A-Chip task: e.g.

- Team Leader
- System Architecture and Algorithm Design Engineer
- Digital VLSI Design Engineer
- Mixed Signal and Analog VLSI Design Engineer
- Chip Physical Layout Design Engineer
- Testability and Testable VLSI Design Engineer
- Integration and Test Engineer
- Advanced Packaging and Thermal Engineer
- VLSI Reliability and Qualification Engineer
- Software Engineer
- Fabrication Service Coordinator



A Practical SOAC Design Flow and Tools: Mentor Graphic + Synopsys + Cadence



Chip Foundry

- Non Radiation Hard Chip Foundry
  - HP, National Semiconductor, etc.
  - Multiproject Chip Fabrication Service through MOSIS
- Radiation-Hard Chip Foundry
  - Industrial: Honeywell Inc.
  - Government: Sandia National Laboratory
  - Research: MIT/Lincoln Laboratory SOI CMOS
- An extended chip foundries survey has been in progress with focus on their technology roadmap which is to be used to define the SOAC future deliveries vision and roadmap.

MIT Lincoln Laboratory SOI CMOS Technology

- MIT/LL SOI CMOS Process Technology: a 0.18 μm gate length, 3-level metal, single Poly, fully depleted SOI CMOS process technology.
- MIT/LL SOI CMOS Multiproject 3rd Fabrication:
  - Design Rule and Model: the version 3.0 design rules and the BSIM3 SPICE model parameters
  - Chip die is limited to the MOSIS tiny chip format (2.3 mm x 2.3 mm) die size.
  - All contributors will be provided with their test die. Functional testing of the device will be the responsibility of the contributor.
  - Important Date: project proposal due April 24, 1998, design due July 31, 1998
  - Contact Person: Dr. Craig Keast, MIT/LL Advanced Silicon Technology Group
  - Source:http://www.ll.mit.edu/AST/mulpage.html
- SOI CMOS vs. Bulk CMOS
  - SOI has an active silicon layer (e.g. 50 nm thickness) with complete oxide isolation. Each transistor is on its own silicon island. Bulk CMOS is diode isolated.
  - SOI allows transistors to be spaced near the minimum lithography dimension. Bulk CMOS requires well and field oxide spacing.
  - SOI has reduced source and drain parasitic capacitance. Fully-depleted SOI design has near ideal subthreshold slope.

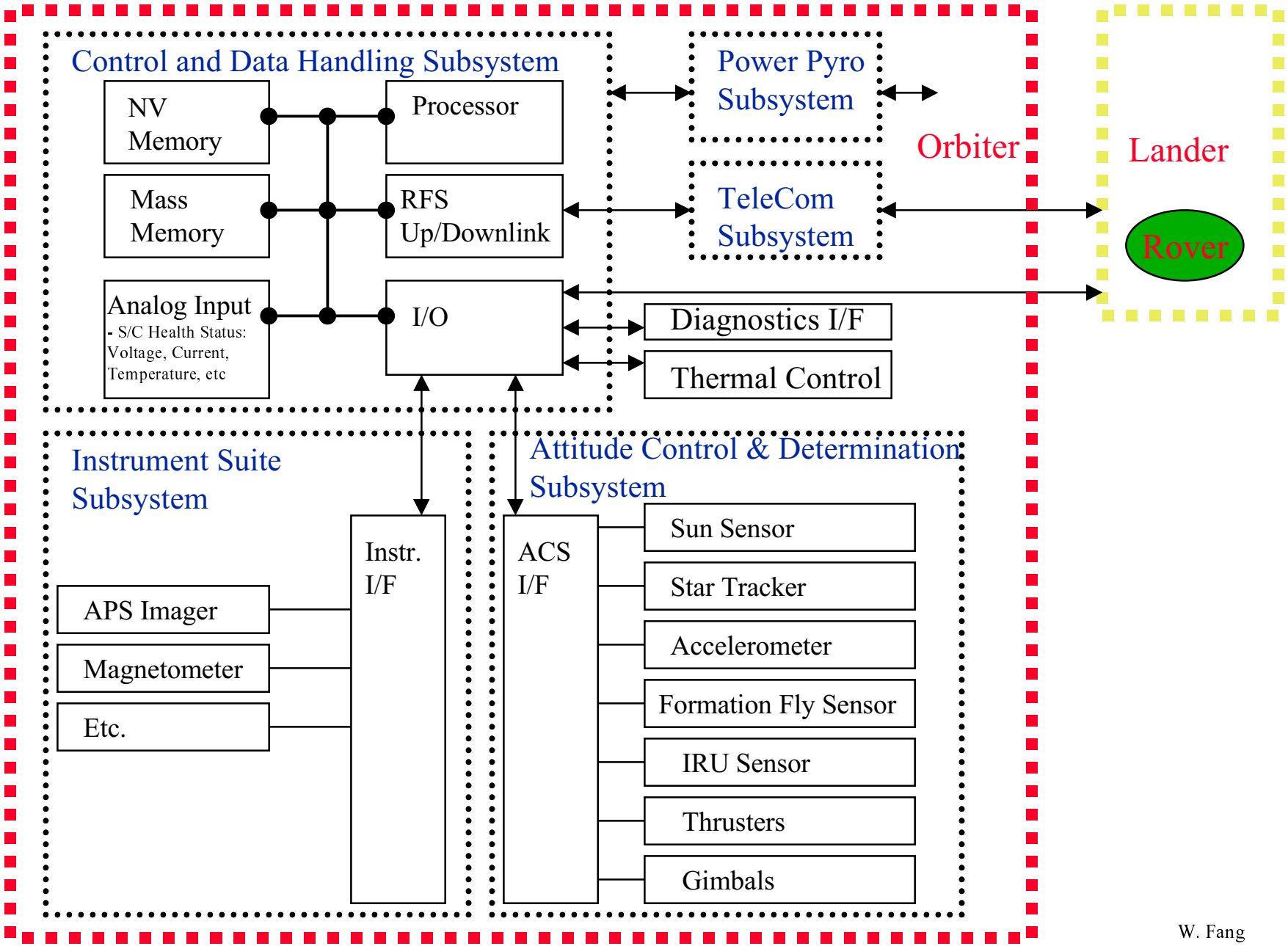
EDA Tools
in the Design Hub

- What is the Design Hub.
  - The Design Hub is a JPL Institutional resource that affords projects access to tools and processes that support detail design, assembly and test phases of a project. It provides work spaces, computers, software tools, network access and remote tele-engineering services (reference: http://dbat.jpl.nasa.gov/dhub/).
- EDA Tools available from the Design Hub
  - A list of current tools can be found in http://dbat.jpl.nasa.gov/dhub/dhubtool.htm
  - e.g. The Mentor Graphics Corp (MGC) EDA Suite of Tools (MGC C.1 release)

  Note that custom chip design tools from Cadence are not available yet as 4-14-98.

- Tool Access Charges:
  - Low CAD tools: $37.57 per month, Mentor Graphics tools: $37.23 per hour, Cadence tools: $45.96 per hour, HP/EEsof tools: $37.89 per hour, Synthesis tools: $65.04 per hour, System tools: $27.43 per hour, MCAD tools A: $19.14 per hour, MCAD thermal: $7.60 per (time card) hour, Hourly Dhub charges: $76.92 per hour

Microspacecraft Configuration
An Example: Comet Sample Return



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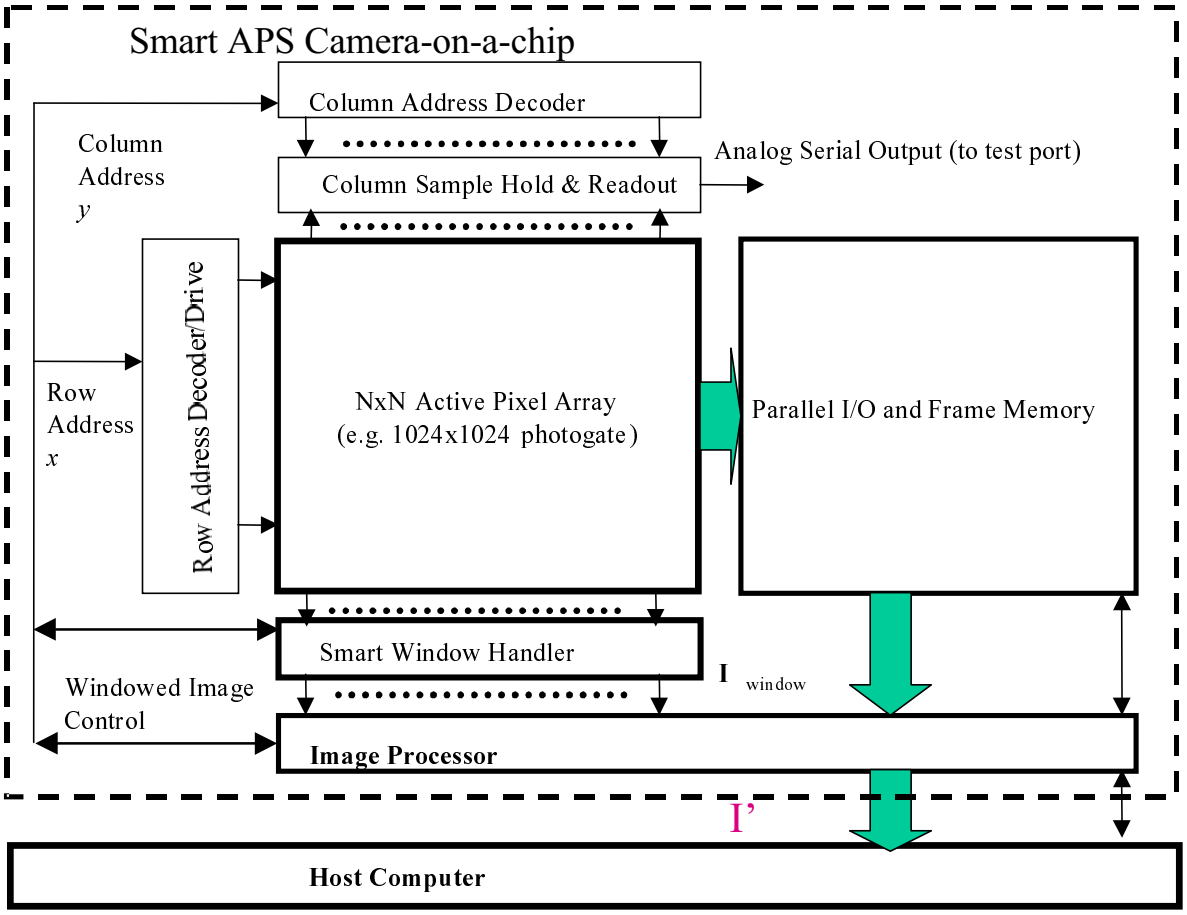
An Experimental Chip: A Smart Camera-on-a-chip

Smart Camera-on-a-chip	Technology: 0.18-micron 0.9-V CMOS		
	Building Blocks	**Size(mm sq.)**	**Power(mW)**
	APS Sensor (1Kx1K)	16	48
	Image Processor	4	40
	Parallel I/O and Frame Memory(1MB)	16	48
	Smart Window Handler	4	40
Total:		40	176



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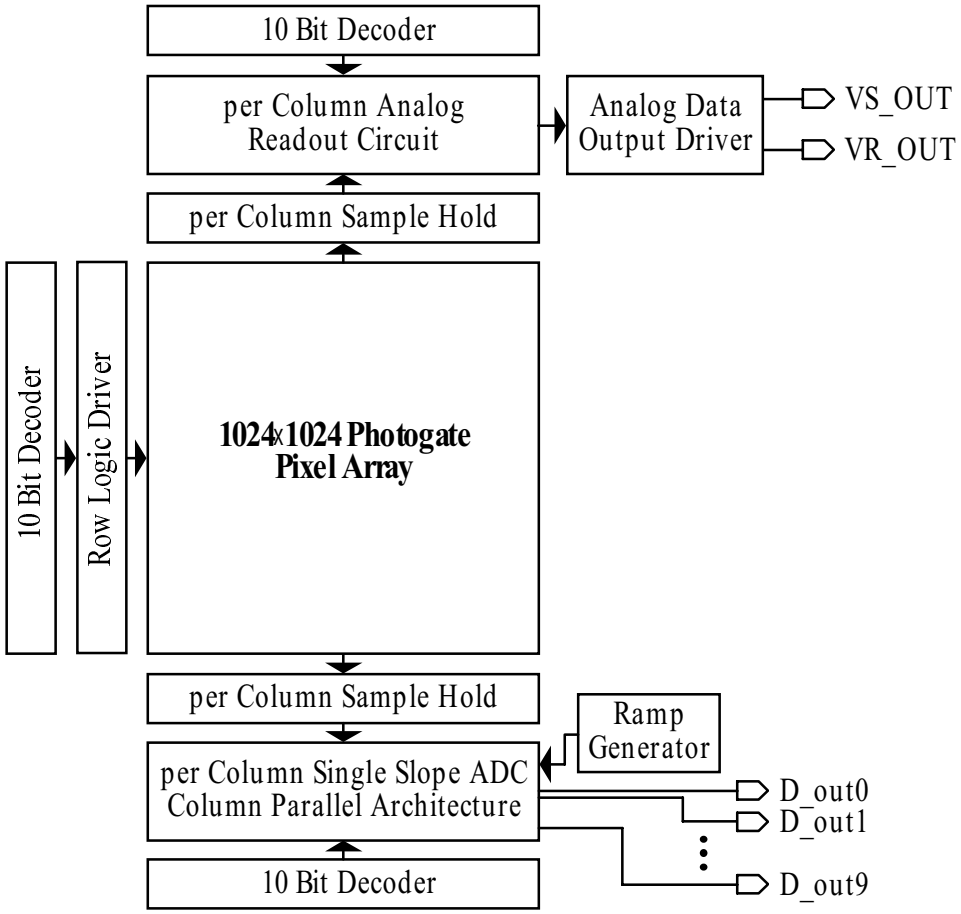
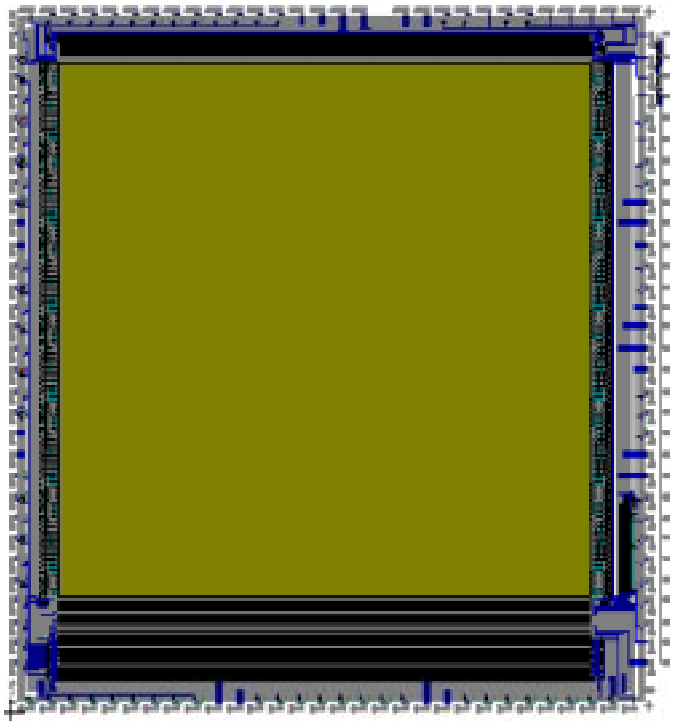
A Prototype APS Camera-on-a-chip

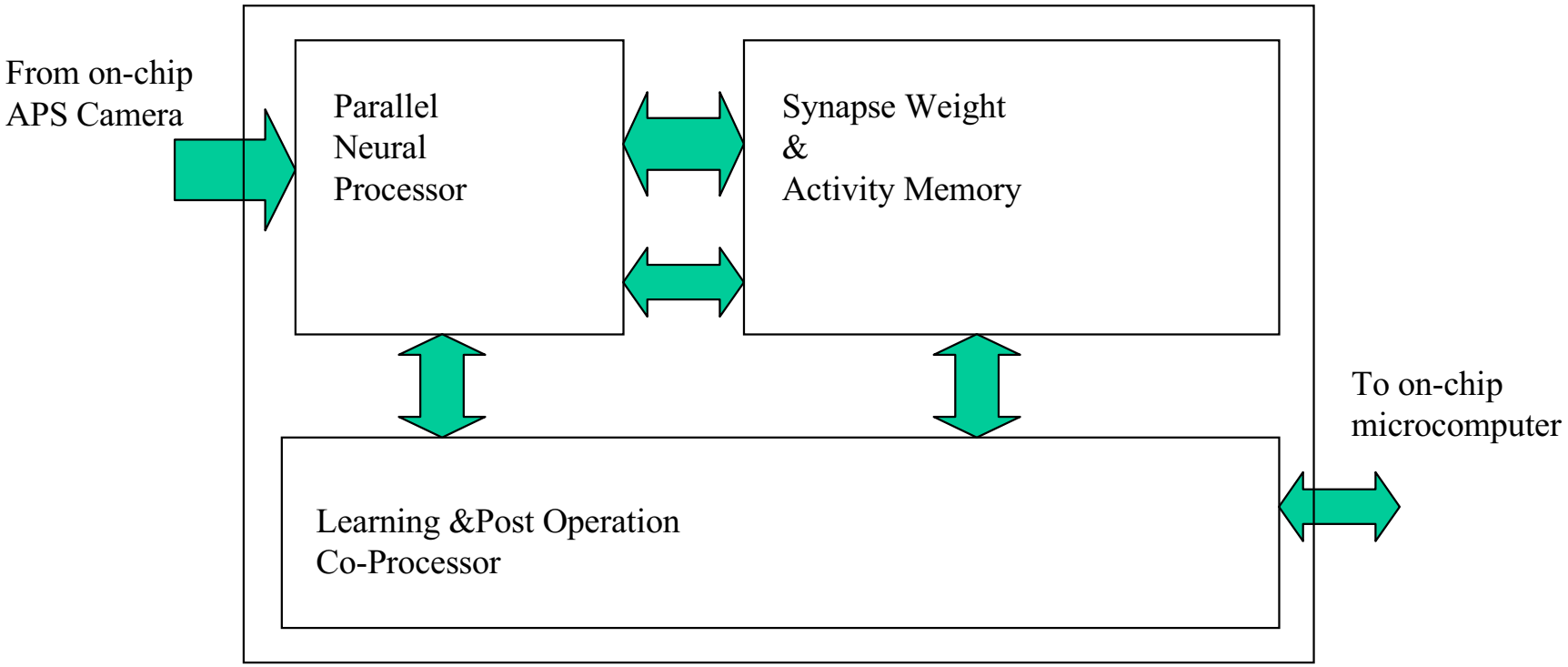


Block diagram of 1Kx1K CMOS APS chip



Layout of 1Kx1K CMOS APS

An Experimental SOAC Chip: A Neurocomputer-on-a-chip



Advanced Neurocomputer-on-a-chip	Technology: 0.18-micron 0.9-V CMOS		
	Neural Processor (1Kx1K or 128x128x64)	64	198
	Neural Processor Controller	4	40
	Post Operation Processor	4	40
	Synapse Memory (1MB)	16	48
	Activity Memory (1 MB)	16	48
	Total:	104	374

Note: A neurocomputer at a size of 128x128 neurons can be implemented in a MIT/LL SOI COM Multiproject 2.3 x2.3 mm tiny chip.

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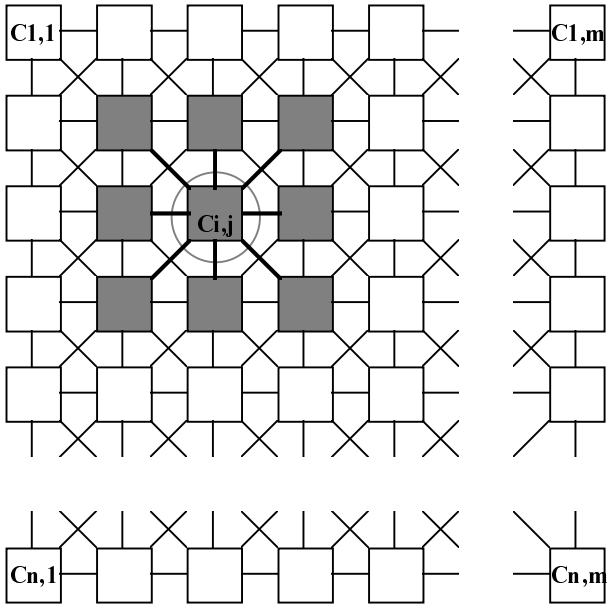
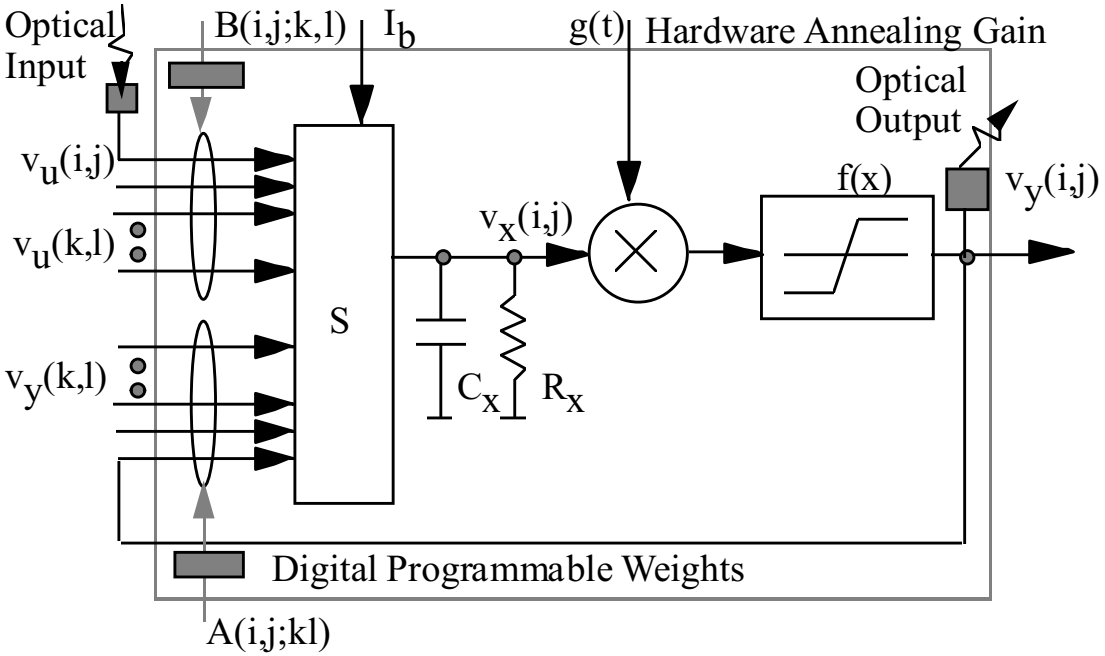
A Prototype CNN Neural Computer-on-a-chip

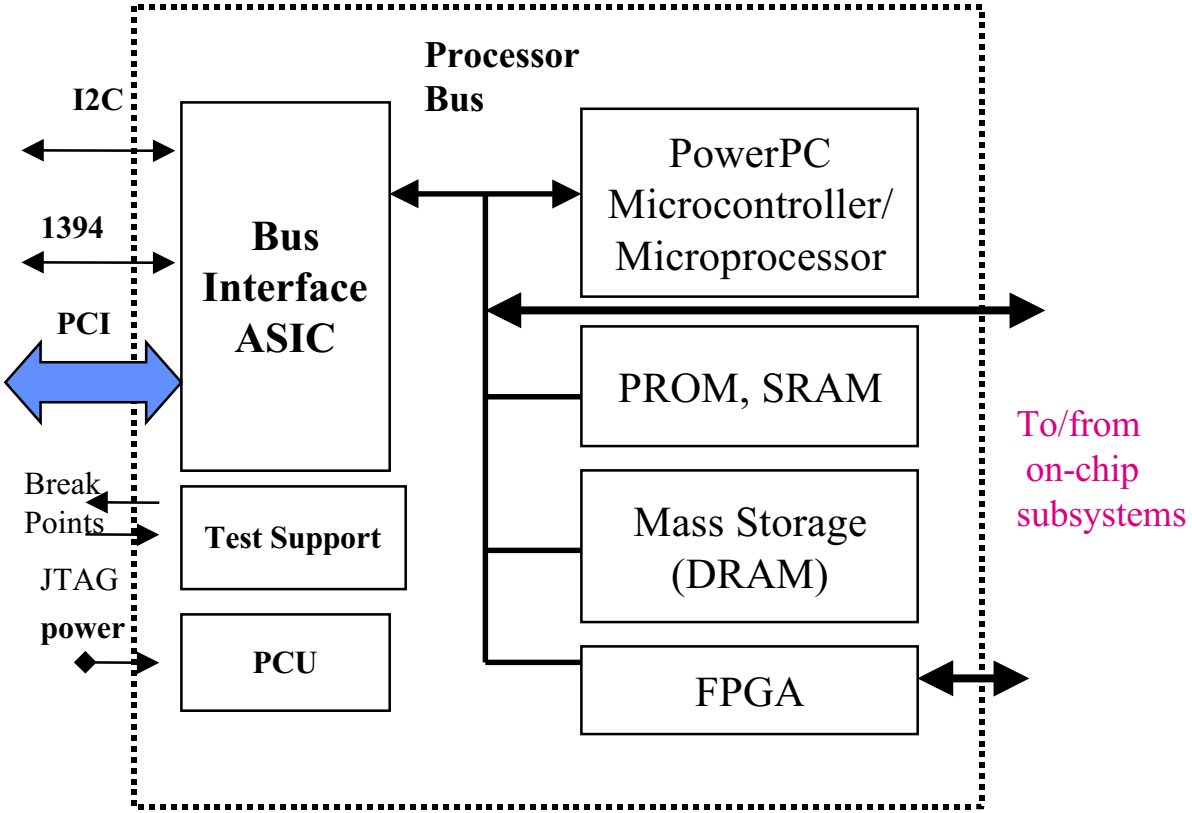




A Neural Computer based on Cellular Neural Network (CNN): An n-by-m CNN on rectangular grid

Functional block diagram of the CNN neuron C(i,j).

An Experimental SOAC Chip: Microcomputer-on-a-chip (leverage from AFC and X2000 1st delivery)



Advanced Microcomputer-on-a-chip	Technology: 0.18-micron 0.9-V CMOS		
	Building Blocks	**Size(mm sq.)**	**Power(mW)**
	PowerPC750 Processor	36	360
	4MB SRAM	64	192
	64 MB DRAM	256	768
	Bus Interface	16	48
	FPGA (256Kgate)	25	250
	Total:	397	1618

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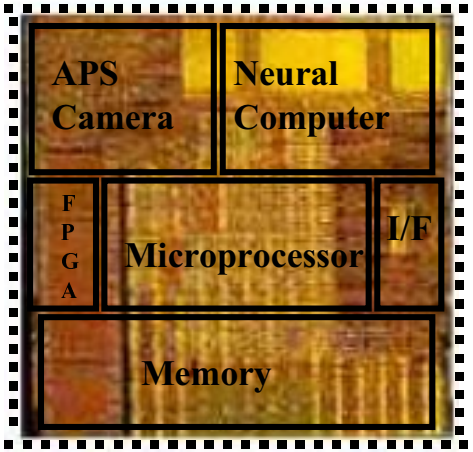
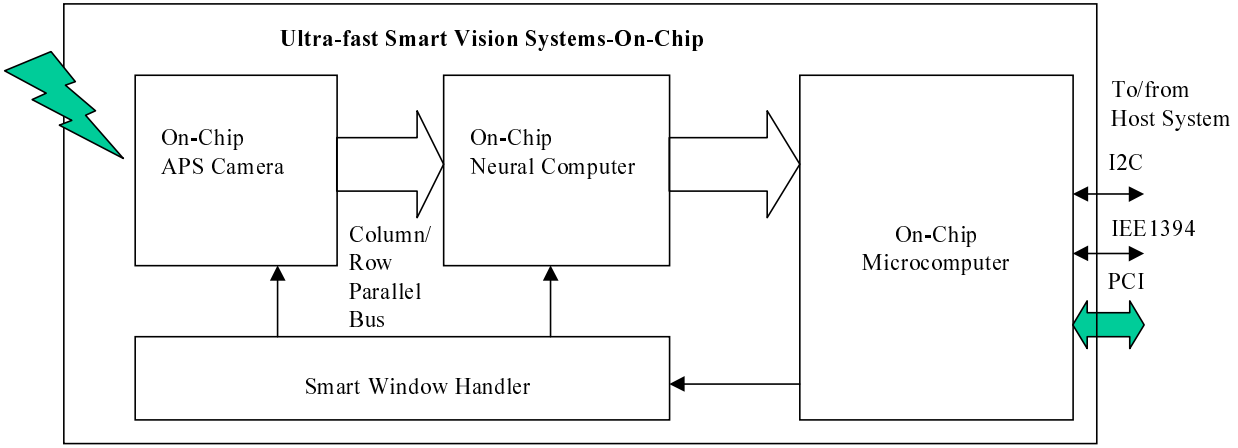
A Next-Generation Experimental SOAC Chip: Smart Vision System





Smart Vision System SOAC	Technology: 0.18-micron 0.9-V CMOS		
On-Chip Subsystems	**Building Blocks**	**Size(mm sq.)**	**Power(mW)**
On-Chip Camera	APS Sensor (1Kx1K)	16	48
	Image Processor	4	40
	Parallel I/O and Frame Memory(1MB)	16	48
	Smart Window Handler	4	40
On-Chip Neural Computer	Neural Processor (1Kx1K or 128x128x64)	64	198
	Neural Processor Controller	4	40
	Post Operation Processor	4	40
	Synapse Memory (1MB)	16	48
	Activity Memory (1 MB)	16	48
On-Chip Microcomputer	PowerPC750 Processor	36	360
	4MB SRAM	64	192
	64 MB DRAM	256	768
	Bus Interface	16	48
	FPGA (256Kgate)	25	250
	Total:	**541**	**2168**
	(86% of a 25x25 mm SOAC chip)		

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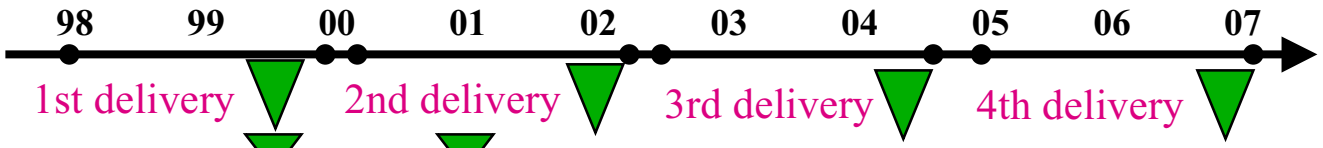
Experimental Chips and SOAC Deliveries Vision

Toward Avionics-on-a-Chip



1. Power-on-a-chip, etc.
=> Power Subsystem SOAC

2. IRU-on-a-chip, etc.
=> ACS Subsystem SOAC

3. Magnetometer-on-a-chip, etc.
4. Camera-on-a-chip, etc.
=> Instrument Subsystem SOAC

5. RFS-on-a-chip, etc.
=> telecomm Subsystem SOAC

6. Neurocomputer-on-a-chip
7. Microcomputer-on-a-chip
8. Microcontroller-on-a-chip
9. Mass Storage-on-a-chip
10. I/O-on-a-chip
=> CDS subsystem SOAC

11. TBD
=> Mission-specific subsystem SOAC

Subsystem SOACs

Avionics SOACs

Smart Vision SOAC

Deep-Submicron technology

0.35 micron 0.18 micron 0.1 micron

Delivery

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Summary

- 1. System integration roadmap

- Refine a detailed roadmap toward avionics on a chip.

- 2. Design method and tool

- Use a pathfinder chip to explore DHUB available tools capability and target fabrications.

- 3. Fabrication survey

- Do an extended fabrication survey to cover Commercial fab. (e.g. National Semiconductor), Industrial Rad-hard (e.g. Honeywell), Research Rad-Hard (MIT LL), etc..

- 4. Experimental chip

- Rafi: deliver a “pathfinder chip” which include digital functions, analog functions, mixed signal functions, and build-in-test design to explore the design and fabrication issues.

- Elizabeth: budget for experimental chip fabrication is available.

- Benny: watch the value of these selected functions and evolve with the SOAC system integration roadmap.

Attendance:

- Wai-Chi Fang, JPL
- Bob Reyaolels (for Ajay Molshe) University of Ankausa
- Rafi Some, JPL
- Benny Toomanan, JPL
- Eilzabeth Kolawa, JPL
- Robert Stirbl, JPL
- Edward Blaze, JPL